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08-23-04

2113

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Pham, Mahn Hung

Serial No.: 09/950,026

Filing Date: September 10, 2001

Title: **Computer System with Improved
Error Detection**§
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Group Art Unit: 2113

Examiner: **Yolanda Wilson**Attny. Docket No. **016295.0693**Client Ref.: **DC-03106**

Mail Stop Response
Commissioner for Patents
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RESPONSE TO OFFICE ACTION DATED April 22, 2004

In response to the Office Action mailed April 22, 2004, Applicants respectfully request reconsideration of the rejections set forth in the Office Action in light of the remarks below.

As the three-month shortened statutory period for reply was due July 22, 2004, Applicants respectfully request a one-month extension of time, with the appropriate fee, to extend the period of reply to August 22, 2004. Therefore, this Response is considered timely filed.

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REMARKS

Claims 1-32 are pending in the present application.

Claim rejection under 35 USC §102:

The Examiner rejected claims 1-5, 7-9, 11-14, 16-21, 23-25, 27-30, and 32 under 35 USC §102(e) as being anticipated by Roohparvar. Applicant respectfully disagrees. Roohparvar is not prior art because the present invention has a conception date prior to the filing date of Roohparvar. Respective declarations signed by Dale Duty, Senior Patent Paralegal at Dell Inc., and Roger Fulghum, the lawyer at the law firm of Baker Botts L.L.P. responsible for preparation and prosecution of patent applications for Dell Inc., are hereby submitted, proving that the conception date of the present application is prior to the effective date of the Roohparvar reference and showing the necessary diligence.

Furthermore, Roohparvar does not anticipate the present invention. The present invention as defined in the independent claims 1, 9, 17 and 25 is related to a computer system with either a plurality of memory module slots which can receive a memory module or to a module within a computer system with a non-volatile memory section. In addition, the present invention requires to record a log in a non-volatile memory section of a memory module.

Roohparvar, on the contrary discloses a single memory chip. Such a single memory chip comprises a random access memory arranged in a matrix. Therefore, the memory device as disclosed by Roohparvar maybe used in a module, however, the necessary steps as defined in the present independent claims will never be performed in a computer system. Roohparvar discloses a single memory devices having redundant memory cells. These redundant cells are used to replace defective memory cells. However, this process is only done during the manufacturing of a memory device as stated in paragraph [0005] of Roohparvar. During such a manufacturing procedure, the memory cell is not part of a memory module. Moreover, the memory device is not part of a computer system. The identification of defective cells is an automated process which is run within the memory device. Once these cells are detected, either a fuse burning process or a laser trimming re-routes the respective signals. Thus, all steps of how the redundant cells are implemented into the memory device are performed

during manufacturing. Roohparvar uses the error code which is stored during such a process in a single register for internal operations only, such as flash memory specific erase routines. After completion of the device, there will be no access to the respective registers for either external read or write access. Thus, a person skilled in the art would never consider Roohparvar as related art.

In addition, Roohparvar does not provide for any means to create and store a log. Per definition, a log includes a plurality of information such as a history of events, etc. Roohparvar merely discloses a portion of a single register for storing an error code which in addition is not retrievable by any external means. As mentioned above, the error code is merely used for internal procedures and defines how specific erase functions of a flash type memory are performed. They do not constitute a log as defined in the present application.

On the contrary, the present invention relates to a computer system with a plurality of memory modules and a unique system of documenting a history of an error occurrence which occurs during the operation of the computer system. Such a history is documented in a log as for example shown in Table II on page 15 of the present application. Even though, the present application also shows the creation and storage of an error code, this is part of a complex log as can be seen, for example, in Table II.

Claim rejection of dependent claims under 35 USC §102 and §103:

In addition, the Examiner rejected the dependent claims 6, 15, 22, 31, 10, and 26 under 35 USC §103(a) as being unpatentable over Roohparvar in view of Lenny. Applicant respectfully disagrees. As pointed out above, the independent claims are not anticipated by the prior art. Thus, all dependent claims include all the limitations of the respective independent claims and are, therefore, patentable at least to the extent of the independent claims. Because the independent claims are clearly not anticipated by the prior art, Applicant would like to defer any discussions with respect to these dependent claims at this point.

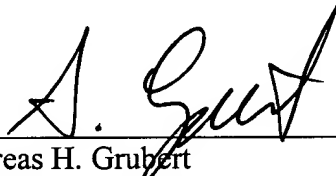
CONCLUSION

The application as defined in the pending claims is patentable under 35 U.S.C. §102 and §103 in view of the cited prior art. Therefore, applicants respectfully request withdrawal of the rejection and allowance of all pending claims.

Applicants do not believe that any other fees are due at this time; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason relating to this document, the Commissioner is authorized to deduct the fees from Deposit Account No. 02-0383, (*formerly Baker & Botts, L.L.P.*) Order Number 016295.0693.

BAKER BOTTS, L.L.P.

Date: August 20, 2004

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